EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(silicide and contacts and CMOS and via and AlCu and (interconnects or interconnection) and temperature). clm.	US-PGPUB; USPAT	OR	ON	2006/05/30 13:23
L2	6444	438/622,627,629,637,687,651.ccls.	US-PGPUB; USPAT	OR	ON	2006/05/30 13:25
L3	5711	2 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2006/05/30 13:25
L6	3193	257/750,751,765,762.ccls.	US-PGPUB; USPAT	OR	ON	2006/05/30 13:25
L7	2785	6 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2006/05/30 13:25
L8	841	7 and (silicide or salicide)	US-PGPUB; USPAT	OR	ON	2006/05/30 13:25
L10	734	8 not 5	US-PGPUB; USPAT	OR	ON	2006/05/30 13:26

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3173	(salicide or silicide) and CMOS and via and (interconnect or metallization)	US-PGPUB; USPAT	OR	ON	2006/05/30 10:10
L2	456	1 and (Al with Cu)	US-PGPUB; USPAT	OR	ON	2006/05/30 10:11
L3	391	2 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2006/05/30 10:46
L4	320	3 and temperature	US-PGPUB; USPAT	OR	ON	2006/05/30 10:46

US-PAT-NO: 6153519

DOCUMENT-IDENTIFIER: US 6153519 A

TITLE: Method of forming a **barrier** layer

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Abstract Text - ABTX (1):

A refractory Metal Nitride and a refractory metal Silicon Nitride layer (64) can be formed using metal organic chemical deposition. More specifically, tantalum nitride (TaN) (64) can be formed by a Chemical Vapor Deposition (CVD) using Ethyltrikis (Diethylamido) Tantalum (ETDET) and ammonia (NH.sub.3). By the inclusion of silane (SiH.sub.4), tantalum silicon nitride (TaSiN) (64) layer can also be formed. Both of these layers can be formed at wafer **temperatures** lower than approximately 400.degree. C. with relatively small amounts of carbon (C) within the film. Therefore, the embodiments of the present invention can be used to form tantalum nitride (TaN) or tantalum silicon nitride (TaSiN) (64) that is relatively conformal and has reasonably good diffusion **barrier** properties.

TITLE - TI (1):

Method of forming a **barrier** layer

Brief Summary Text - BSTX (2):

The present invention relates generally to the processing of semiconductor devices, and more specifically to providing a diffusion **barrier** onto a semiconductor device.

Brief Summary Text - BSTX (4):

Modern semiconductor devices are requiring speeds in excess of 200 megahertz. In order to form future generations of semiconductor devices, copper (Cu) will essentially be required for **interconnects**. One problem with the use of copper is that copper cannot directly contact silicon dioxide because copper diffuses too easily through the silicon dioxide layer. Therefore, in the prior art the copper is typically surrounded by a diffusion **barrier** on all sides.

Brief Summary Text - BSTX (5):

Diffusion **barriers** for copper include a number of materials, such as silicon

nitride and various refractory metal nitrides (TiN, TaN, WN, MoN) and refractory silicon nitrides (TiSiN, TaSiN, WSiN), or refractory metal-semiconductor-nitride layers. Of all of these **barriers,** the two showing promise for **barriers** include tantalum nitride (TaN) and tantalum silicon nitride (TaSiN). These materials are usually deposited by sputtering. However, sputtering generally has poor sidewall step coverage, where step coverage is defined to be the percentage of a layer being deposited on a specific surface divided by the thickness of a layer being deposited on the uppermost surface of a semiconductor device. In the case of sputtered tantalum nitride (TaN) and tantalum silicon nitride (TaSiN), and the step coverage for a 0.35 .mu.m **via** can be in the range of 5% to 20% for an aspect ratio of 3:1. Such low step coverage increases the risk that the **barrier** material will not be thick enough to be an effective diffusion **barrier** along the sides and bottom of a deep opening. In an attempt to get enough of the material along the walls of openings, a much thicker layer at the uppermost surface is deposited, however, this is undesirable because it increases the resistance of the **interconnect**.

Brief Summary Text - BSTX (6):

Chemical vapor deposition (CVD) has been used to form tantalum nitride. The precursors for TaN includes tantalum halides, such as Tantalum Pentachloride (TaCl.sub.5). The problem with tantalum halides is that the halides react with the copper causing **interconnect** corrosion. Another precursor includes penta[dimethylamido]tantalum (Ta(NMe.sub.2).sub.5). When this precursor is used to deposit tantalum nitride (TaN), the compound that is actually forms is an insulating layer of Ta.sub.3 N.sub.5. An insulator cannot be used in contact openings or **via** openings because the insulator prevents electrical contact between the upper **interconnect** layer and the lower **interconnect** layer.

Brief Summary Text - BSTX (7):

Still another known precursor includes terbutylimido-tris-diethyl amino tantalum [(TBTDET), Ta.dbd.NBu(NEt.sub.2).sub.3]. This compound can be used to form TaN. However, there are problems associated with this precursor. Specifically, deposition **temperatures** higher than 600.degree. C. is needed to deposit reasonably low resistivity films. Such high **temperatures** for back-end **metallization** are incompatible for low-k dielectrics and also induces high stresses due to thermal mismatch between the back-end materials. Another problem with the TBTDET precursor is that too much carbon (C) is incorporated within the layer. This compound generally has approximately 25 atomic percent carbon. The relatively high carbon content makes the layer highly resistive, and results in films that are less dense, lowering the diffusion **barrier** effectiveness for a comparable thickness of other materials. The resistivity of TaN when deposited using TBTDET at **temperatures** lower than 600.degree. C.

is approximately 12,000 .mu.ohm-cm. Films with such a high resistivity (desired is less than approximately 1000 .mu.ohm-cm) cannot be used for making effective **interconnect** structures.

Brief Summary Text - BSTX (8):

CVD of titanium silicon nitride (TiSiN) has been demonstrated using titanium tetrachloride (TiCl.sub.4). This compound is again undesirable because in forming the TiSiN, chlorine is once again present which causes corrosion of copper and other materials used for **interconnect**.

Brief Summary Text - BSTX (9):

A need, therefore, exists to deposit a TaN or TaSiN using organometallic precursors that can be formed relatively conformally with a reasonable resistivity and good **barrier** properties at lower wafer **temperatures**.

Drawing Description Text - DRTX (4):

FIG. 2 includes an illustration of a cross-sectional view of FIG. 1 after forming materials needed to form **interconnects** in accordance with one embodiment of the present invention;

Drawing Description Text - DRTX (5):

FIG. 3 includes an illustration of a substrate of FIG. 2 after forming inlaid **interconnects** to doped regions within the substrate;

Drawing Description Text - DRTX (7):

FIG. 5 includes an illustration of a cross-sectional view of the substrate of FIG. 4 illustrating the opening to the lower **interconnect**;

Drawing Description Text - DRTX (8):

FIG. 6 includes an illustration of a cross-sectional view of the substrate of FIG. 5 after forming an **interconnect** to a lower **interconnect** level; and

Detailed Description Text - DETX (3):

A refractory Metal Nitride and a refractory metal Silicon Nitride layer are formed using metal organic chemical deposition. More specifically, tantalum nitride (TaN) can be formed by a Chemical Vapor Deposition (CVD) using Ethyltrikis (Diethylamido) Tantalum [(ETDET), (Et.sub.2 N).sub.3 Ta.dbd.NEt] and ammonia (NH.sub.3). By the inclusion of a semiconductor source such as silane (SiH.sub.4), a tantalum silicon nitride (TaSiN) layer can also be formed. Both of these layers can be formed at wafer **temperatures** lower than 500.degree. Celsius with relatively small amounts of carbon (C) within the film. Therefore, the embodiments of the present invention can be used to form

tantalum nitride (TaN) or tantalum silicon nitride (TaSiN) layer that is relatively conformal and has reasonably good diffusion **barrier** properties.

Detailed Description Text - DETX (5):

Tantalum nitride (TaN) and tantalum silicon nitride (TaSiN) are formed using ETDET/NH.sub.3, and ETDET/NH.sub.3 /SiH.sub.4 respectively. For TaN, the deposition generally takes place in a CVD reactor at a pressure in the range of 5-15 Torr. The monitored deposition **temperature** varies depending upon where the **temperature** is being monitored. If the heater block **temperature** is being monitored, the **temperature** is generally in a range of approximately 400-480.degree. Celsius. If the wafer **temperature** is measured, the **temperature** is typically in a range of approximately 350-400.degree. C.

Detailed Description Text - DETX (6):

The ETDET is introduced using Helium (He) as a carrier gas that is bubbled through the ampoule. The flow rate of the Helium (He) is in the range of 200-800 sccm. The heater box **temperature** for the ampoule is maintained at approximately 80.degree. Celsius. In general, the heater box **temperature** can be maintained within a range of approximately 50-90.degree. Celsius. The **temperature** of the ETDET within the ampoule is approximately about 10.degree. Celsius lower than the heater box **temperature**. Ammonia (NH.sub.3) is introduced at a rate ranging from 200-500 sccm which generally gives a deposition rate of approximately 150-200 .ANG./minute The deposition rate will also depend on the reactor configuration. Using these parameters TaN film can be deposited that has less than 15% carbon (C) and is generally no more than 1%. When used as a **barrier** layer, the layer TaN is usually deposited to a thickness in a range of approximately 200-300 .ANG. along an exposed surface of the substrate, and generally has step coverage of greater than 50% at the bottom surface of an opening having an aspect ratios of 3:1.

Detailed Description Text - DETX (7):

The flow of ammonia has been observed to enhance the deposition across all **temperature** ranges. Without ammonia limited or no deposition is observed even at high wafer **temperatures**. This is in contrast to the precursor (TBTDET) used to deposit TaN as reported in literature, which reported deposition without ammonia (NH.sub.3).

Detailed Description Text - DETX (8):

In CVD systems, there is typically more difficulty depositing the layer at the bottom of the opening, and therefore, the step coverage at the bottom is a good indicator of the thinnest portion of the film. The TaN also has been found to have reasonably good adhesion to the surfaces of both metals and

oxides. This is important for integrating the layer into an **interconnect** process. Should the layer be used to make contact (electrical or physical) to a Silicon containing layer such as a gate electrode or doped regions within a semiconductor substrate, titanium may be deposited between the TaN and Silicon (Si) to form a good ohmic contact. Without the titanium, a relatively high contact resistance between TaN and p+ Silicon may be formed because of large differences in the work functions between p+ silicon and tantalum nitride.

Detailed Description Text - DETX (10):

Different source gases may be used for the Silicon source and the TaN precursor. Specifically, it is possible that Disilane (Si.sub.2 H.sub.6) or some other Silicon gas could be used. In addition, it is believed that source gasses containing other semiconducotr souces, such as germanium will work as well. However, care should be exercised, in assuring that gas phase reaction is not present. Also, the wafer **temperature** of the deposition should not exceed 500.degree. Celsius, and be typically less than 400.degree. Celsius, because of the issues noted previously. The TaN precursor has similar concerns. In general, the ethyl group attached to the doubly bonded nitrogen can comprise either an ethyl [(Et.sub.2 N).sub.3 Ta.dbd.NEt] or a methyl [(Et.sub.2 N).sub.3 Ta.dbd.NMe] group. The carrier gas for the ampoule includes helium (He), argon (Ar), nitrogen (N.sub.2) or hydrogen (H.sub.2).

Detailed Description Text - DETX (12):

Embodiments of the present invention are better understood with the example that follows in which two levels of **interconnects** are formed using the chemically vapor deposited material. FIG. 1 includes an illustration of a cross-sectional view of a portion of a semiconductor device substrate 10 before **interconnects** are formed. The semiconductor device substrate 10 is a monocrystalline semiconductor wafer, a semiconductor-on-insulating wafer, or any other substrate used to form semiconductor devices. Field isolation regions 12 are formed over the semiconductor device substrate 10. Doped regions 14 are source/drain regions for a transistor and lie within the substrate 10 adjacent to the field isolation regions 12. A gate dielectric layer 22 and gate electrode 24 overlie the substrate 10 and portions of the doped regions 14. An interlevel dielectric layer 26 is deposited over the semiconductor device substrate 10. The interlevel dielectric layer 26 can include an undoped, a doped, or combination of doped and undoped silicon dioxide films. In one particular embodiment, an undoped silicon dioxide film is covered by a borophosphosilicate glass (BPSG) layer. After planarization of layer 26, openings 28 are formed through the interlevel dielectric layer 26 and extend to the doped regions 14. As illustrated in FIG. 1, the openings 28 include a contact portion which is relatively narrow that contacts the doped

regions 14, and a relatively wider **interconnect** trench, which is where the **interconnect** is formed. In one example of FIG. 1, the contact portion has an aspect ratio is 3:1 as compared to the trench. This is an example of a dual damascene process for forming inlaid **interconnects** which are generally known within the prior art.

Detailed Description Text - DETX (13):

The materials used to form the contacts and **interconnects** are then deposited over the interlevel dielectric layer 26 and within the openings 28. As illustrated in FIG. 3, which illustrates a partially completed device, layer 32 of titanium or other refractory material is formed, and is in contact with the doped regions 14. This layer generally has a thickness in a range of approximately 100-400 .ANG.. Next, a TaN or TaSiN layer 34 is formed over layer 32. The tantalum nitride layer 34 or TaSiN layer 34 is formed using the previously described deposition parameters. The thickness of the layer is in the range of approximately 200 to 300 .ANG.. A conductive layer 36 is formed within the remaining portions of the openings and overlying 34. The conductive layer 36 typically includes copper (**Cu**), aluminum (**Al**), tungsten (W) or the like. In this particular embodiment, the conductive layer 36 is copper. The partially completed device is then polished to remove the portions of layers 32, 34 and 36 that overlie the interlevel dielectric layer 26. This forms contact portions and **interconnect** portions for the **interconnects** 44 and 42 as illustrated in FIG. 3.

Detailed Description Text - DETX (14):

A second interlevel dielectric layer 56 is deposited and patterned over the **interconnects** 42 and 44 and the first interlevel dielectric layer 26. FIGS. 4 and 5 illustrate top and cross-sectional views, respectively, of the second interlevel dielectric layer after patterning. The second interlevel dielectric layer 56 includes a doped or undoped oxide. The patterning forms a **via** opening 52 and an **interconnect** trench 54. Other **via** openings and **interconnect** trenches are formed but are not shown in FIGS. 4 and 5.

Detailed Description Text - DETX (15):

As illustrated in FIG. 6, TaN or TaSiN layer 64 is then deposited using one of the previously described deposition techniques. Layer 64 contacts the lower **interconnect** 42. Layer 64 has a thickness in a range of approximately 200 to 300 .ANG. and is covered by a second conductive layer 66 using a material similar to layer 36. The portions of the layers 64 and 66 overlying the second interlevel dielectric layer outside of the **interconnect** trench are then removed by polishing to give the structure as illustrated in FIG. 6. The combination of layers 64 and 66 forms a bit line 62 for the semiconductor device. A

substantially completed device 70 is formed after depositing a passivation layer 72 overlying the second level **interconnects,** as illustrated in FIG. 7. In other embodiments, other insulating layers and **interconnects** levels can be formed but are not shown in the figures.

Detailed Description Text - DETX (16):

Many benefits exist for embodiments of the present invention. The CVD reaction that forms TaN or TaSiN is performed at wafer **temperatures** lower than approximately 500.degree. Celsius, and typically less than 400.degree. Celsius. Therefore, the process is compatible with low-k dielectrics and does not induce high stresses in the films. The amount of carbon incorporation is less than 15 atomic percent, and typically 1 atomic % or less. Therefore, the film does not have porous qualities and is a better diffusion **barrier** compared to using TBTDET as a precursor. The reduced carbon results in a resistivity of the CVD TaN films that are at least an order of magnitude lower compared to the prior art use of the TBTDET. Still, other advantages with the embodiments is the relative ease of integration into an existing process flow.

Detailed Description Text - DETX (17):

Thus it is apparent that there has been provided, in accordance with the invention, a process for depositing a diffusion **barrier** to fabricate a semiconductor device, which fully meets the advantages set forth above. Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications as fall within the scope of the appended claims and equivalents thereof.

Claims Text - CLTX (1):

1. A method of forming a **barrier** layer comprising the steps of:

Claims Text - CLTX (16):

the step of reacting is performed at a substrate **temperature** of no greater than approximately 400.degree. Celsius.

Claims Text - CLTX (17):

8. The method of claim 1, wherein the **barrier** layer is deposited using a plasma.

Claims Text - CLTX (20):

bubbling the carrier gas through the metal organic precursor, wherein the ampoule includes the metal organic precursor and a heater having a **temperature** of approximately 50.degree. Celsius to approximately 90.degree. Celsius.

Claims Text - CLTX (21):
10. A method of forming a **barrier** layer comprising the steps of:

Claims Text - CLTX (34):
maintaining a wafer **temperature** of less than approximately 400.degree. Celsius.

Claims Text - CLTX (35):
15. The method of claim 14, wherein the **barrier** layer is deposited using a plasma.

Claims Text - CLTX (40):
forming an **interconnect** within the opening, wherein the **interconnect** is formed by:

Claims Text - CLTX (55):
26. The method of claim 1, wherein the **barrier** layer is part of an **interconnect**.

Claims Text - CLTX (56):
27. The method of claim 10, wherein the **barrier** layer is part of an **interconnect**.

Other Reference Publication - OREF (1):
M.H. Tsai et al., "Metal-organic chemical vapor deposition of tantalum nitride **barrier** layers for ULSI applications", XP 000595265, Thin Solid Films 270(1995) 531-536, pp. 531-536.

Other Reference Publication - OREF (2):
Paul Martin Smith et al., "Chemical Vapor Deposition of Ternary Refractory Nitrides for Diffusion **Barrier** Applications", XP-002123863, Jun. 1996 VMIC Conf. (ISMIC), pp. 162-167.

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Sun, et al.; "Diffusion **Barrier** Properties of CVED Tantalum Nitride for Aluminum and Copper Interconnections"; VMIC Conf; 1995 ISMIC; pp. 157-62.

Other Reference Publication - OREF (5):

Tsai, et al. Metalorganic chemical vapor deposition of tantalum nitrid by tertbutylimidortis (diethylamido) tantalum for advanced **metalization**; Appl Phys Lett 67 (8); pp. 1128-130; (1995).

Other Reference Publication - OREF (8):
Akasaka et al.; "Low-Resistivity Poly-Metal Gate Electrode Durable for High-**Temperature** Processing"; IEEE Transactions on Electron Devices; vol. 43, No. 11; pp. 1864-68; (1996).

Other Reference Publication - OREF (11):
Sun, et al."A Comparative Study of CVD Tin and CVD TaN Diffusion **Barriers** for Copper Interconnection"; IEEE 1995 Int'l Electron Devices Meeting Technical Digest; pp. 461-64 (1995).

Other Reference Publication - OREF (12):
Kasai, et al.;"W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron **CMOS** LSIs"; IEDM; pp. 497-500 (1994).

Other Reference Publication - OREF (13):
Reid, et al.; Evaluation of amorphous (Mo, Ta, W)-Si-N diffusion **barriers** for <Si>ICu metallizations; Thin Solid Films, vol. 236; pp. 319-24; (1993).

Other Reference Publication - OREF (14):
Wang, et al.; "Diffusion **barrier** study on TaSix and TaSixNy"; Thin Solid Films,; vol. 235; pp. 169-74 (1993).

Other Reference Publication - OREF (18):
Chiou, et al.; "Microstructure and Properties of Multilayer-Derived Tungsten **Silicide**"; Journal of Electronic Materials, vol. 16; No. 4; pp. 251-55 (1987).